CSR 5302 (IICD531)

Electronic Design Automation (1)

李炯霆 (JT Li)

Spring 2026

Contributed by many professors, such as

台灣大學電機系 張耀文　清華大學電機系 黃錫瑜

交通大學資科系 李毅郎　中央大學電機系 劉建男

元智大學資工系 林榮彬,

台灣大學 Ric Huang, Roland Jiang,

and many others

教育部　超大型積體電路與系統設計教育改進計畫　EDA聯盟

Acknowledgement

- Besides materials from**教育部,** all other data/pictures/videos were obtained from public web sites, talks & webinars
  - Such as academy (Stanford, UT Austin, UCB, George Tech., …), Synopsys, Cadence, Siemens(Mentor), Ansys, Altium, …
  - Also thank Raul Camposano, Antun Domic, Patrick Groeneveld (who teach EE292A in Stanford) for their courtesy
  - And Tung-Chieh Chen

- I am deeply indebted to Professor Ernest Kuh for his mentorship and unwavering guidance

Logistics

- **Time/Location: Monday (14:20–17:20) @LRB教室**
- **Instructor:** JT Li (e-mail: jtli@mx.nthu.edu.tw, j_t_li@hotmail.com**)**
  - Office: 綜三, 4th Floor, room C07 (Phone #: +886-9-8131-7373)
  - Office Hour: Monday before and after the class, or by appointment
- **Teaching Assistants** – (__)

- **Prerequisites:** logic design & data structures (& basic transistor design)
- **Reference:**
  - S. H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 1999
  - Y.-W. Chang, K.-T. Cheng, L.-T. Wang (editors): *Electronic Design Automation: Synthesis, Verification, and Test*, Elservier, 2009
  - https://bjpcjp.github.io/pdfs/chips/VLSI-design-automation.pdf (Naveed A. Sherwani)
  - LOGIC SYNTHESIS AND VERIFICATION ALGORITHMS (Gary D. Hachtel, Fabio Somenzi)

https://eclass.uth.gr/modules/document/file.php/E-CE_U_104/Practical_Problems_in_VLSI_Physical_Design_Automation.pdf
Sung Kyu Lim

Course Info (1)

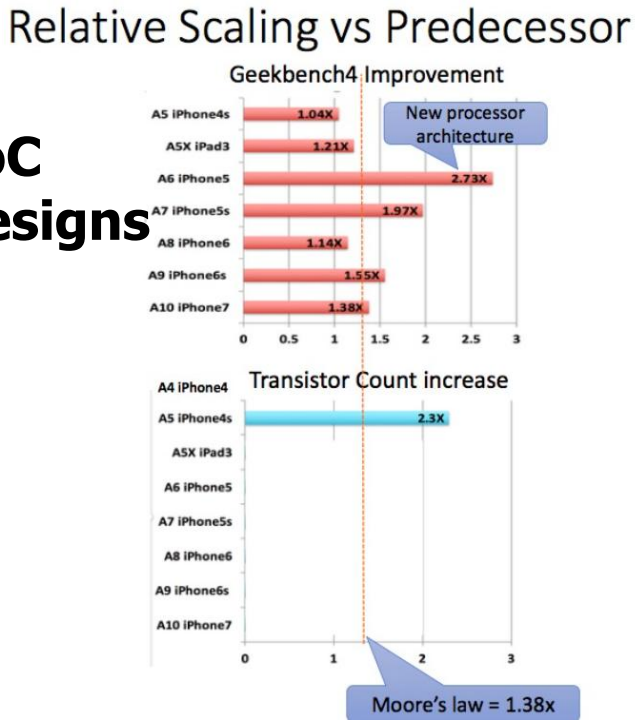
- **Course Objectives:**
  - Understand what EDA is all about – very broad area
  - This semester is more for digital SoC designs
  - Study several important algorithms used in physical design
  - Motivate interests - Many software talents are needed in EDA
  - Learn problem formulation and solving by designing algorithms
    → can expand to other areas

Welcome questions!
They will make us to understand more clearly

iPhone Processors

EDA plays a critical role!

SoC Designs



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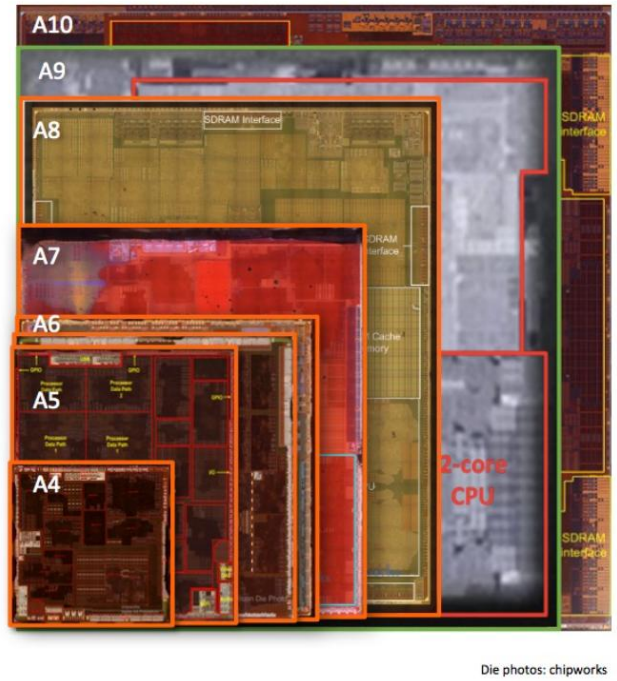
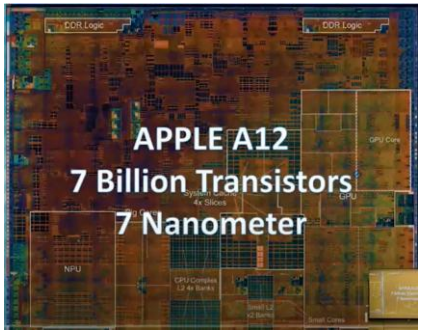


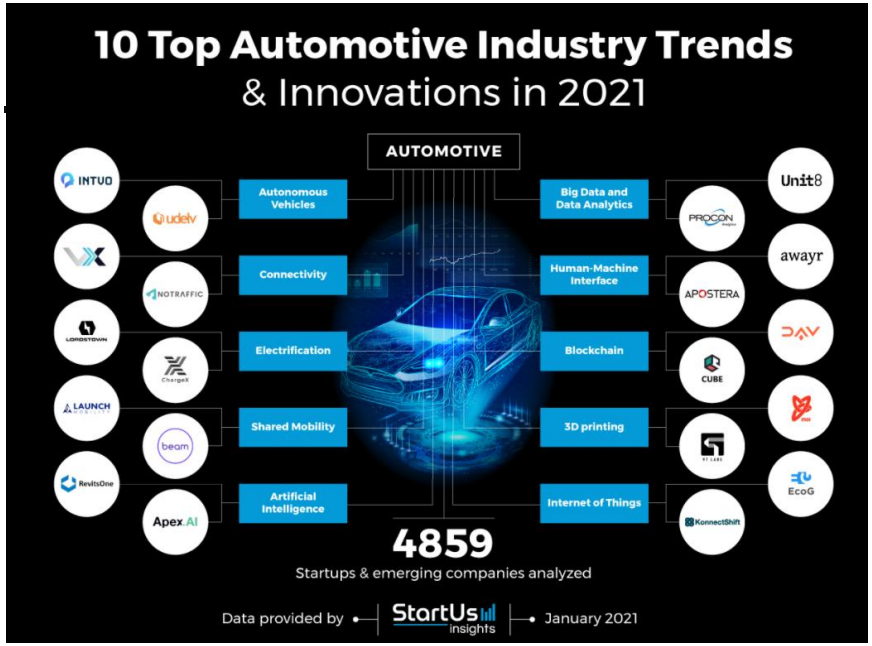
Die photos: chipworks

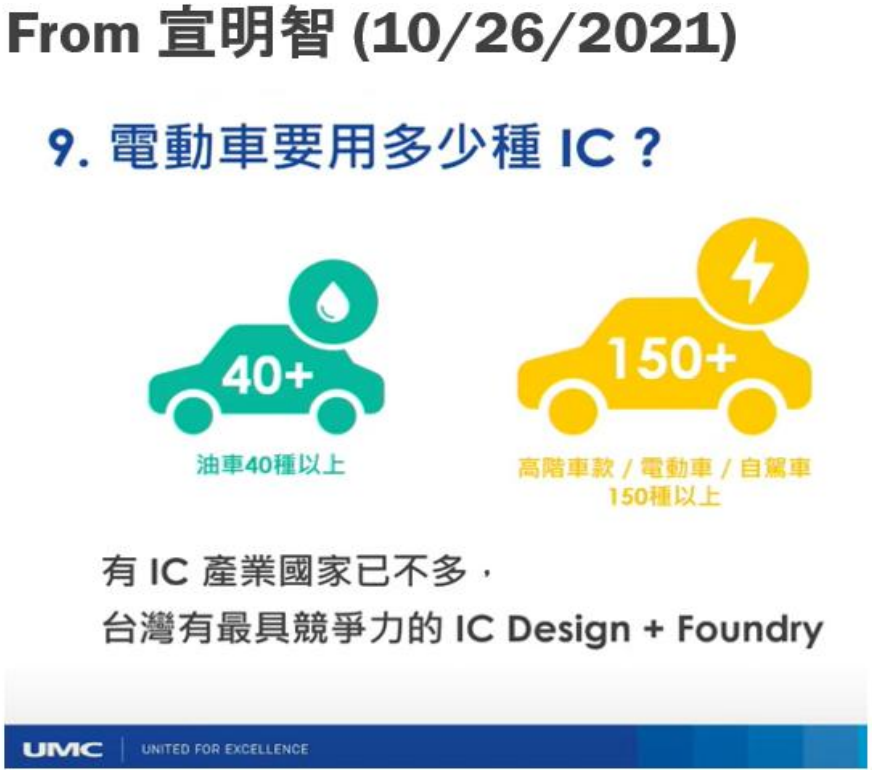
Chips getting bigger

- **How to synthesize?**
- **How to place?**
- **How to route?**
- **DRC/LVS?**
- **RC extraction?**
- **How to fix timing?**
- **Database**
- **ECO (Engineering Change Order)**
- **…**



Apple's A15 Bionic chip powers iPhone 13 with 15 billion transistors, new graphics and AI (@5nm)





- Electronics market for auto is big
  - Many custom design components!
  - May not need to use the most advanced 3nm technology?
  - Need lots of simulations, customized PDKs, …

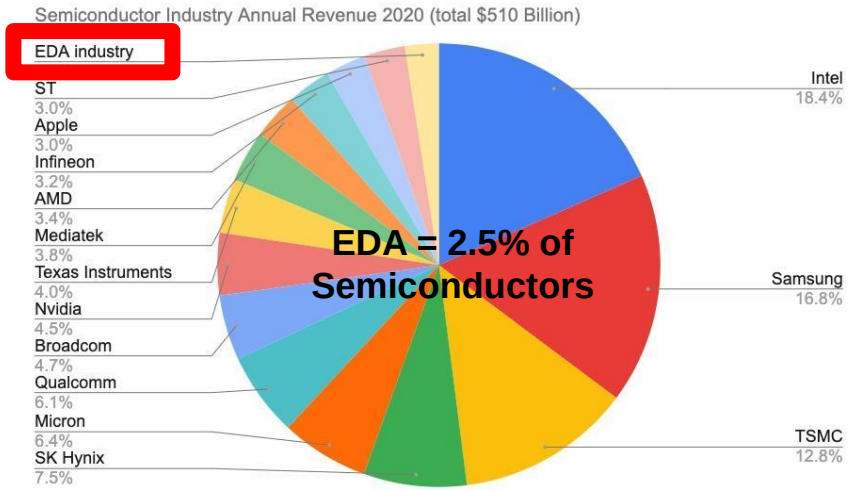
EDA also plays a critical role!

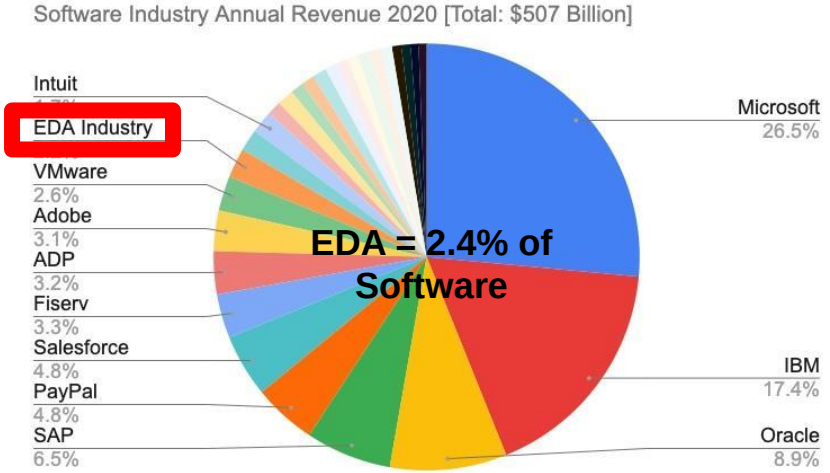
EDA Industry: Semiconductor + Software

~2017

Company	Employees	Annual Sales	Market value	Major Locations, next to Silicon Valley
Synopsys	15,000	$3.7B	$52B	India, China, Europe, Armenia, Taiwan
Cadence	10,000	$2.7B	$50B	India, China, Europe, Taiwan
Siemens EDA (Mentor)	~6,000	~$1.6B	~$20B	Oregon, India
Other EDA	~20,000	~$2B	$10B	Worldwide
Total EDA approx.	**50,000**	**$10B**	**$132B**	Worldwide

Semiconductor companies





Software companies

2024: total semi $650B;
EDA: ~16B

Semiconductor Design 101 Course

What is EDA?

Prof. David Pan

- Acronym for *Electronic Design Automation*
- A **crucial** market segment consisting of software, hardware, IP, and services for the definition, planning, design, implementation, verification, and subsequent manufacturing of semiconductor devices, or **chips**

- "EDA is at the **heart** of the **heart** of modern information technology" – Dr. Aart de Geus, co-founder and executive chair of Synopsys
- No EDA ➔ No chip or semiconductor industry as we know of today!

- EDA market size: $16 billions in 2024
- Semiconductor industry: $628 billion in 2024
- Global IT industry: $11.7 trillion in 2024
- Global GDP: $110 trillion in 2024

Chip Design / EDA is not for Fainted Heart

- Modern chips are "systems-on-chip" -- integrating many different components to a single chip
  - Digital: CPU, GPU, memory, control logic, …
  - Analog, RF, Sensors, and mixed-signal
- Deal with unbelievable complexities
  - Billions of transistors & 100's km wiring, in your nail size!
- Very expensive to tapeout (e.g., $50M in 5nm) – verify, verify!
- Dedicated fabs (TSMC, Globalfoundries, …)
- Fabless companies (Nvidia, AMD, Qualcomm, Broadcom, …)
- Handshaking through process-design-kit (PDK) – complicated too!

- To deal with such extreme complexity ➔ **divide and conquer**

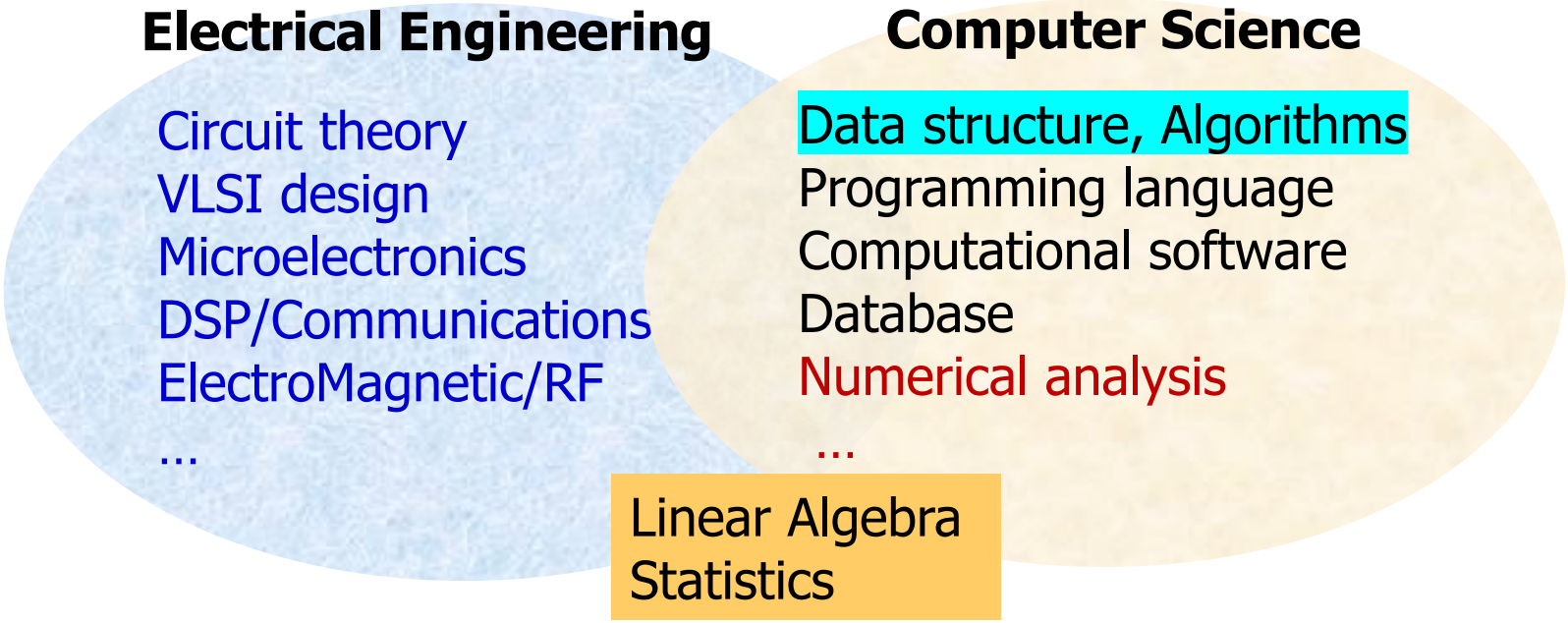
EDA Ecosystem

- Includes EDA software, tools, and methods from specifications to tapeouts (with various abstraction layers to deal with complexity)
  - Design tools
  - Simulation tools
  - Verification tools
- Digital, analog, mixed-signal, RF, packaging, PCB
- Design for manufacturability, reliability, security, …
- Intellectual Property (IP) reuse - do not reinvent the wheel!

- EDA is highly interdisciplinary (EE, CS, Math, Physics, AI, …), thus a PhD degree will never be treated as "over-qualified" ☺
- If you master EDA, you can do any job (software engineer, hardware engineer, chip designer, AI, or Wall Street, …) ☺

Introduction Of EDA

- EDA – where HW and SW meet each other → Productivity



- EDA is concerned about HW/SW design in terms of
  - Correctness
  - Productivity
  - Optimality
  - Scalability

Cadence CEO Anirudh Devgan said EDA is CS + Math (+ EE)

Why EDA Tool Development Is Exciting

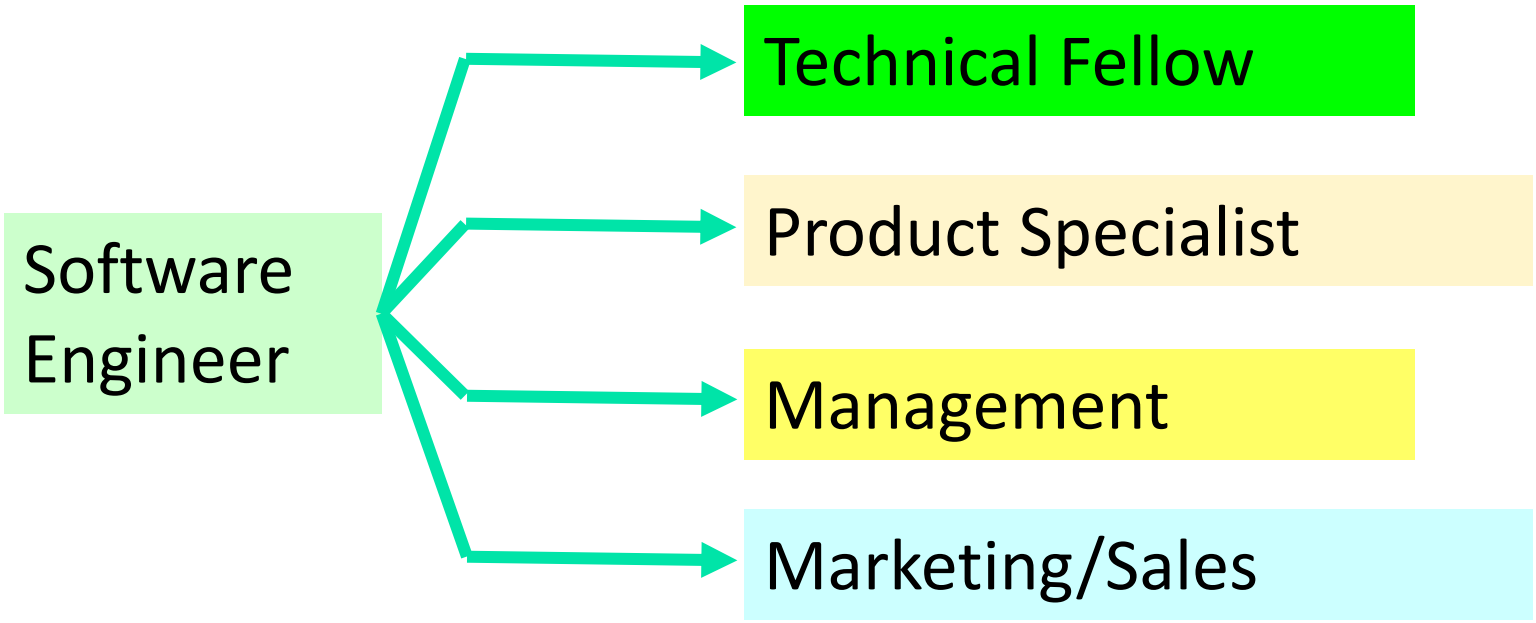
- Many problems to solve & improve
  - Tool performance leaps and bounds
  - Good to have competitors – can't stand still
- A multidisciplinary area
  - Programming, IC design & manufacturing, math, compute environment, statistics, physics, …
- Very stimulating
- Customers' problems often surprise you

Customers pay you and say "Thank you", if you indeed solve their problems.

The new trends often require many current methods to be re-thought, re-implemented

I guess pay is not bad ☺
Next are examples of job description

Career Growth Path



SYNOPSYS®

Staff R&D Engineer-8014

General Information

Job Title: Staff R&D Engineer-8014

City: Sunnyvale

Date Posted: 26-Nov-2024

Job Subcategory: R&D Engineering

Remote Eligible: No

Job ID: 8014

State/Province: California

Job Category: Engineering

Hire Type: Employee

Base Salary Range: $138000 - $207000

What You'll Need:

- Proficiency in C++ development.
- Experience with static timing analysis, digital design / VLSI flow. Knowledge of synthesis / P&R optimization techniques is a plus.
- Knowledge of AI and machine learning techniques.
- Strong understanding of electronics and circuit design.
- Excellent written and verbal communication skills.

You will be part of a dynamic and innovative team responsible for getting the best quality of results with tight runtime and memory budgets for our flagship Fusion Compiler and ICC Compiler II products.

https://technews.tw/2024/06/30/how-to-get-a-job-at-nvidia/

必備扎實技術基礎

輝達全球招募副總裁杜蘭強調，輝達要找的人要有強大數理背景，求職者一定要擅長某技術領域，或有某領域專業知識：機器學習、人工智慧、電腦視覺化、程式設計、深度學習演算法、資料處理或GPU應用等。

匿名工程師也強調，必須具扎實數據結構（**data structures**）**與演算法**知識，因輝達最初幾輪面試，**寫Code**等技術測驗占相當高比例，也會為之後面試大大加分。專業技術測驗不僅是要解決問題，還是展現邏輯思維與拆解複雜難題的機會。

別怕開口，善用內部推薦

用「STAR原則」描述工作經歷

能自信且有條理將之前工作經歷對面試官侃侃而談，是成功的關鍵。匿名工程師說，面試官很看重求職者「**說故事的能力**」，因此應多在履歷或自我介紹運用「STAR原則」：Situation（情境）、Task（任務）、Action（行動）、Result（結果），好好描述個人故事。

了解公司文化和團隊

展現特色，但避免過度自信

接受失敗並持續成長

EDA for Digital SoC

Verification

Pre-layout
Post-layout

Implementation

Physical Design

Spring 2026

EDA for Custom/Analog Designs

Verification
Pre-layout
Post-layout
(DRC, RC, IR-Drop, Spice)

Implementation

Physical Design

Fall 2026

Packaging/3DIC

Physical
Implementation

Multiphysics
Analysis

(For Tsing Hua Univ.)

Course Info (2)

- **Course Outline**
  - Introduction to EDA; technology nodes; basic CMOS design (1 week)
  - Algorithms, graph and complexity (1 week)
  - Physical design: compaction, floorplan, placement, routing (6 wks)
    - Gordian placer example
  - Logic synthesis, optimization, technology mapping (2 weeks)
  - Mid term quiz (date - TBD)
  - Timing, delay calculation, clock tree synthesis, simulation (2 week)
  - Program demo/presentation (1 week)
  - Design rules, nanometer design (if we have time)
  - HsinPo Wang

Course Info (3)

- **Grading**
  - 18% homework
    - Discussion encouraged, but solutions are written down individually
  - 60% programs & demo/presentation (team work of <=2 persons)
    - Especially for global router
  - 12% mid term quiz (open notes, no wifi search)
  - 10% for class participation (e.g., asking questions, demo, helping)

(Note: final grade is based on grading on a curve)

Homework, Programs, Presentation, Exam

- Homework (18%)

Hw-1:
- Logic equ. & gates
- Algorithms about searching

Hw-2:
- Truth table, BDD

Hw-3:
- Floorplan representation
- B* tree for packing
- Partitioning

- Mid term exam (12%)

- Participation (10%)

- Program (60%)

Need to write reports on some procedures

Prog-1 (20%)
- Bring up CUDD, run Boolean examples
- (equivalence checking, technology mapping)

Prog-2 (20%)
- Bring up quadratic placers (Gordian, RePlace) (Github, may need to use Visual Studio, welcome to build OpenRoad)

Prog-3 (20%)
- Develop a global router (2D), demo