

# Bibliography

- [1] Shekhar Borkar, "Low Power Challenges for the Decade", *Proceedings of the conference on Asia South Pacific Design Automation Conference*, 2001.
- [2] A. P. Chandrakasan and R. W. Brodersen, "Minimizing Power Consumption in Digital CMOS Circuits", *Proceedings of the IEEE*, 1995.
- [3] Liqiong Wei, Zhanping Chen, Mark Johnson and Kaushik Roy, "Design and Optimization of Low Voltage High Performance Dual Threshold CMOS Circuits", *Proceedings of the 35th annual conference on Design automation conference*, 1998.
- [4] Vijay Sundararajan and Keshab K. Parhi, "Low Power Synthesis of Dual Threshold Voltage CMOS VLSI Circuits", *Proceedings of 1999 international symposium on Low power electronics and design*, 1999.
- [5] Nikhil Tripathi, Amit Bhosle, Debasis Samanta and Ajit Pal, "Optimal Assignment of High Threshold Voltage for Synthesizing Dual Threshold

- CMOS Circuits”, *The 14th International Conference on VLSI Design*, 2001.
- [6] Yen-Te, and TingTing Hwang, ”Low Power Design Using Dual Threshold Voltages”, *Proceedings of ASP-DAC 2004*, pp. 205-208, Japan, Jan. 2004.
- [7] Yutaka Tamiya, ”Performance Optimization Using Separator Sets”, *Proceedings of ICCAD 1999*, pp. 191-194, 1999.
- [8] David Nguyen, Abhijit Davare, Michael Orshansky, David Chinnery, Brandon Thompson, and Kurt Keutzer, ”Minimization of Dynamic and Static Power Through Joint Assignment of Threshold Voltages and Sizing Optimization”, *Proceedings of ISLPED*, 2003.
- [9] Predictive Technology Model  
”<http://www-device.eecs.berkeley.edu/~ptm/>”.